MODELING OF RADIATION INDUCED BURNOUT IN DMOS TRANSISTORS

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ABSTRACT

One of the major problems that hinders the utilization of n-channel DMOS transistors in radiation environments is their susceptibility to prompt gamma radiation. At high dose rates, the electron-hole pairs generated result in large photocurrents that can lead to second breakdown which can result in device burnout, at voltages well below rated breakdown. In this paper, results of time-dependent two-dimensional numerical simulations of this effect are presented. In addition, the effect of different process and design parameters on the failure mechanism initiating burnout are examined. The simulation results provide the physical insight necessary to incorporate process and structure modifications in order to improve the radiation tolerance of the device. Experimental results are used to corroborate the simulation results.

INTRODUCTION

DMOS transistors offer quite attractive features for power applications, such as power regulation and DC-DC conversion, both as discrete devices or as part of a Power Integrated Circuit (PIC). However, n-channel DMOS transistors are known to be susceptible to burnout in transient radiation environment [1-4]. When the device is in the off state, transient ionizing radiations generate electron-hole pairs. Large photocurrents can turn on the parasitic npn bipolar transistor shown in Figure 1. Previous work [1-3] has shown that the injected electron current from the emitter of the npn transistor can lead to, photocurrent-stimulated, Current Induced Avalanche CIA followed by thermal runaway and eventually to device burnout.

Modeling of prompt gamma radiation induced burnout in DMOS transistors is needed to enable dose rate radiation hardened process and device development [4-5]. In this paper the results of two-dimensional, time-dependent, numerical simulations of this effect are presented. Also, the effects of applied drain voltage and different process and design parameters such as p-body sheet resistance, n^+ source length and drain doping profile are examined for their effect on the radiation induced failure mechanism with the aim to improve the radiation tolerance of the device. These simulation results are used to gain more physical insight to understand the failure mechanism. This is necessary in order to improve the radiation tolerance of the device; because, a good understanding is required if solutions incorporating process and device structure modifications are to be realized. Experimental results obtained using dielectrically isolated test devices corroborate the simulation results.

RESULTS AND DISCUSSION

Transient analysis was performed using the in-house computer program PADRE [6]. The program solves the Poisson and current continuity equations. It takes into account relevant physical phenomena such as avalanche multiplication and dependence of mobility on field and doping concentration. An ionizing radiation burst is modeled as a pulse with zero rise and fall times. During the radiation pulse, additional electron-hole pairs are generated at a constant rate of 4.3e13 e-h pairs/cm^3/rad.

Figure 2 shows the electron current vectors of a DMOS transistor simulated at t=1.7 nsec during receiving a gamma dot pulse of 30 nsec width and a dose rate of 3 e10 rad(Si)/sec. The device is in the off-state with drain-source voltage V_{DS}=125V and gate-source voltage V_{GS}=0. It is shown that the n^+ source injects electrons into the p-body and n^- drift region. This is because the photocurrent generated causes a voltage drop along the p-body region which forms the base of a parasitic npn transistor in the device. When the voltage drop across the n^+/p-body junction exceeds about 0.6V, the injected electron current increases significantly. Figure 3 shows the electron and hole distribution along the cross section xx' at t=1.7 nsec. The electron and hole densities in the drift region are shown to be nearly equal and both are larger than the background doping (5e14cm^{-3}). This phenomenon indicates that the device operates in the high injection region. Under such conditions the depletion region expands towards the n^-/n^+ drain junction. Therefore, the field distribution is modified and the peak field shifts from the the p-body /n^- junction to the n^+/n^- high-low junction. This effect can be seen in Figure 4 where the field intensity is plotted along the cross section xx' at t=0 , 1.7 and 22 nsec. The peak field intensity at t=22nsec (20v/μm) is high enough to cause avalanche injection.

Figure 5 shows the photocurrent response of a device biased at V_{DS}=125V and exposed to a 3e10 rad(Si)/sec ionizing pulse of 30nsec duration. The slope change (dI/dt) of the

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drain current at turn on is indicative of the initial primary photocurrent leading to a secondary photocurrent resulting from the turn on of the n^+/p-body junction. It is also shown that the drain current continues to increase and that the npn transistor is in a self sustained mode for t>30nsec. In this mode a feedback loop is established and when its gain attains unity, the current supplied by avalanche injection keeps the n^+/p-body junction turned on which causes second breakdown leading to device failure.

To examine the effect of drain bias, V_{DS} was decreased to 110V. The resulting response is shown in Figure 6 (curve A) and is of particular interest. In this case, the loop gain does not reach unity; and therefore, the drain current starts to decay at the end of the ionizing pulse. It is noted that at t=30nsec there is a sudden drop in the drain current Id followed by a slower decay. This drop corresponds to the cessation of the radiation pulse and the charge redistribution within the device. This is followed by a slower decay governed by carrier recombination in the conductivity modulated regions. As the level of injected minority carriers decrease below the doping level, current decays at a faster rate. To consider the effect of the parasitic npn transistor on the failure mechanism, the n^+ source was removed from the doping profile. The resulting diode was simulated under the same bias and radiation conditions as the device in Figure 5 and its photocurrent response is shown in Figure 6 (curve B). It should be noted that the device does not breakdown and the drop in current at t=30nsec is equivalent to the prompt drop component of the DMOS transistor's current response (curve A).

The effect of the heavily doped substrate is examined by removing the n^+ layer at the drain contact from the device shown in Figure 1. Figure 7 shows the field distribution at t=30 nsec for a device subjected to the same bias and radiation exposure conditions as that of Figure 4. The peak field (15v/μm) is insufficient to cause avalanche current and burnout is prevented at a dose rate of 3e10(rad(Si)/sec. This is in agreement with reported experimental results [2].

The effect of p-body sheet resistance was also investigated. It is anticipated that lower p-body sheet resistance will reduce the gain of the parasitic npn transistor and the feedback loop. Thus, lower peak currents result at the same applied bias and radiation exposure conditions. Figure 8 shows the electron concentration and electric field distribution, along the cross section xx', at t=30nsec, for a device with lower p-body sheet resistance than that of Figures 3 and 4. This device is biased at V_{DS}=125V and exposed to a 3e10 rad(Si)/sec pulse. It is clear that the injected electron current is greatly reduced because of the reduction in the npn bipolar transistor gain.

The injected electron current from the n^+ source can be reduced by minimizing the overlap of n^+ source and p-body. Figure 9 shows the electron current vectors of a device with shorter n^+ (reduced lateral width) source than that of Figure 2. Since the voltage drop along the the junction is less, the electron current injected is insufficient to cause device burnout.

This analysis provides the means to predict the onset of burnout which is important to evaluate the prompt gamma radiation hardness of various designs. The above results are in agreement with previous work [1-2] and supports the observation that reducing the gain of the parasitic npn transistor and preventing the onset of avalanche injection will increase the radiation tolerance of the DMOS transistor.

To corroborate the simulations, test DMOS transistors were fabricated using the Dielectrically Isolated Bipolar-CMOS-DMOS (BCDMOS) technology [7] in both 8 and 14 ohm.cm tubs. Devices were fabricated with the following parameter variations: the n^+ source diffusions shortened and lower p-body sheet resistance.

DMOS transistors were characterized under different dose rate stresses and bias conditions. Radiation testing was performed using both a high-powered Linear Accelerator (LINAC) and a flash x-ray. Testing was carried out under worst case bias condition, namely with both gate and source grounded and a positive voltage applied to the drain. Figure 10 shows a typical photocurrent response versus time for a device that burnt out, where V_{DS}=250V and subjected to a dose rate of 2.3e10 rads(Si)/sec, with pulse duration of 30 nsec. Figure 11 shows the peak photocurrent versus dose rate for a device biased at V_{DS}=125V. Also shown are the experimental and simulation threshold peak currents. The experimental results show that devices with standard n^+ source and biased at 125V burnout at a dose rate of 3e10 rad(Si)/sec, whereas those biased at 110V do not burnout. Also, it was demonstrated that devices with a short n^+ source do not burnout under the same bias and dose rate conditions. This is in agreement with the simulation results.

CONCLUSION

Results of time-dependent two-dimensional numerical simulations of prompt gamma radiation effect on DMOS transistors have been presented. The effects of different process and design parameters such as p-body sheet resistance, n^+ source length and drain doping profile on the burnout failure mechanism have been examined. The simulation results provide the physical insight necessary to incorporate process and structure modifications to improve the radiation tolerance of the device. Finally, the analysis provides the means to help predict the onset of radiation induced burnout in order evaluate the prompt gamma radiation hardness of various designs.

ACKNOWLEDGEMENTS

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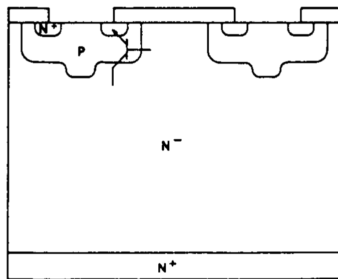

Figure 1: Schematic diagram of a DMOS transistor.

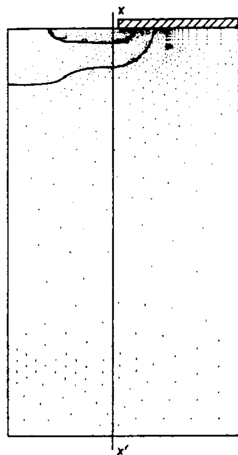

Figure 2: Electron current vectors a DMOS transistor simulated after 1.7 nsec of excitation, V_{DS}=125V and γ=3e10 rad(Si)/sec.

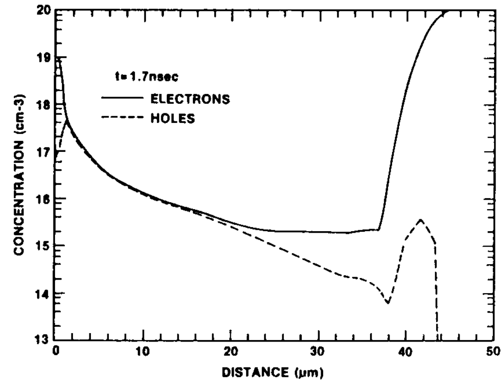

Figure 3: Electron and hole distributions along xx' at t=1.7 nsec.

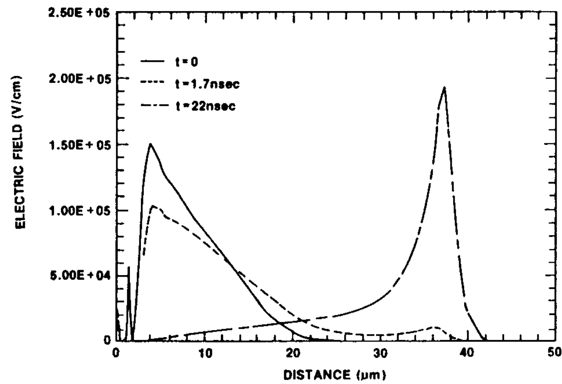

Figure 4: The field intensity along xx' at t=0, 1.7 and 22 nsec, γ=3e10 rad (Si)/sec.

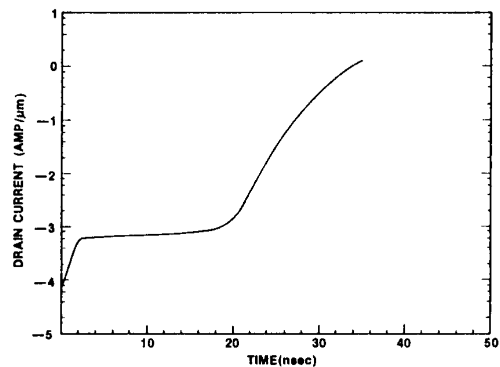

Figure 5: Drain current versus time of a DMOS transistor, V_{DS}=125V, γ=3e10 rad (Si)/sec and pulse width=30 nsec.

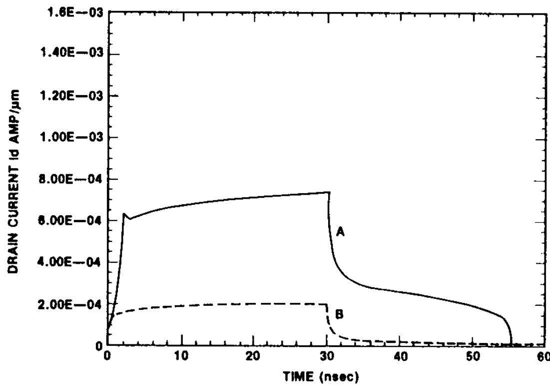

Figure 6: Photocurrent response of a DMOS transistor (curve A), V_{DS}=110V and a corresponding diode (curve B) V_{DS}=125V with γ=3e10 rad (Si)/sec and pulse width=30 nsec.

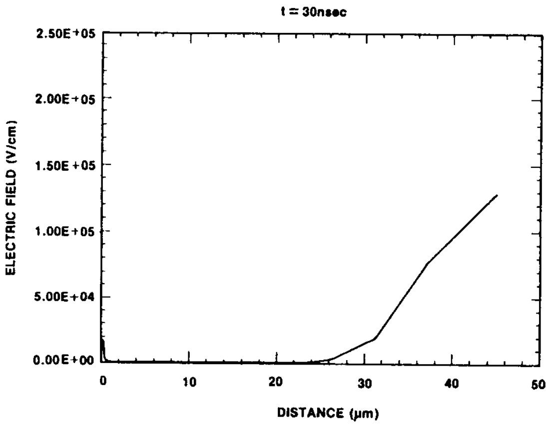

Figure 7: Electric field distribution along xx' for a DMOS transistor without n^+ substrate at t=30 nsec, V_{DS}=125V, γ=3e10 rad(Si)/sec. and pulse width =30 nsec.

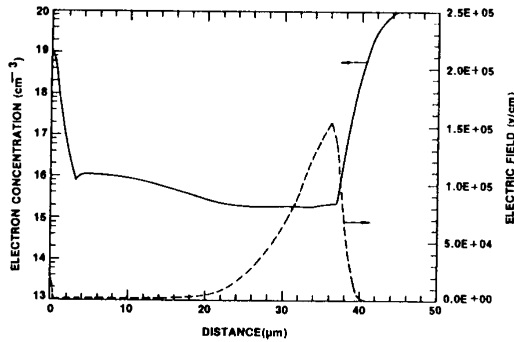

Figure 8: Electron concentration and electric field distribution along xx' at t=30 nsec for a device with a low p-body sheet resistance.

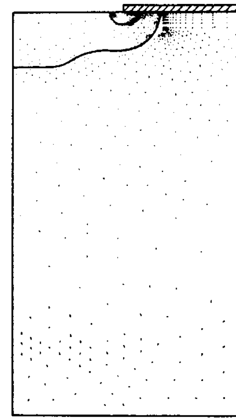

Figure 9: Electron current vectors for a DMOS transistor with a shorter n^+ source at t=30 nsec. V_{DS}=125V, γ=3e10 rad(Si)/sec and pulse width =30 nsec.

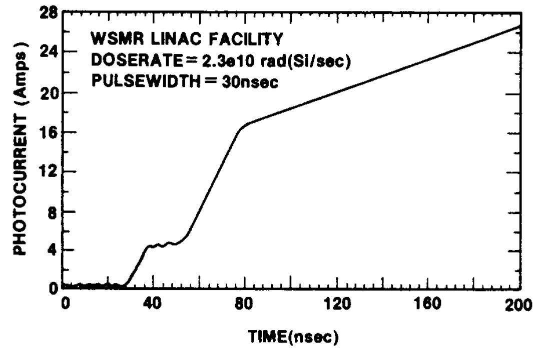

Figure 10: Measured peak current versus time of a DMOS transistor V_{DS}=250V and γ=2.3e10 rad (Si)/sec.

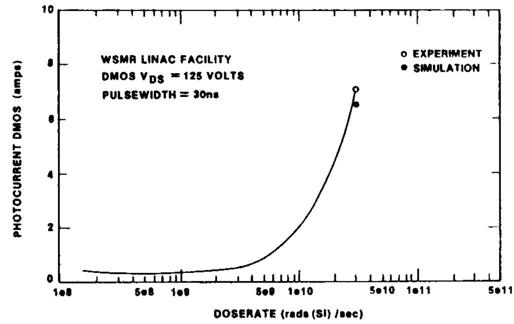

Figure 11: Measured peak current versus dose rate of a DMOS transistor V_{DS} = 125V. O measured and ● simulation threshold peak currents.