Development of Long-Range UHF-band RFID Tag chip Using Schottky Diodes in Standard CMOS Technology

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Abstract — **We present the design of three key building blocks for UHF-band passive RFID tag chip, i.e., voltage multiplier, ASK demodulator, and internal clock generator. An analysis on a simple equivalent circuit of RFID tag chip for long reading range is presented taking into account the finite turn-on voltage of tag chip. The Schottky diodes used in the passive RFID tag chip were fabricated using Titanium (Ti/Al/Ta/Al)-Silicon (n-type) junction in 0.35 µm CMOS process, and the effect of size of Schottky diode on the turn-on voltage and the input impedance of the voltage multiplier was investigated. For 300 mV RF input voltage, the fabricated voltage multiplier using Schottky diodes generated output voltages of 1.5 V and corresponding voltage conversion efficiency of 45%. In addition, we propose an example circuit for internal oscillator of tag chip with digital calibration, which can generate precise copy of RFID reader timing signals.**

Index Terms — **RFID, Schottky diodes, CMOS, ASK demodulator, oscillator with calibration, voltage multiplier.**

I. INTRODUCTION

The radio frequency identification (RFID) are growing rapidly with a good deal of promising features in technology and applications, especially in the UHF band for its suitability in the middle to long range communication link between a reader and tag [1].

Considering volume production at lowest cost, the fabrication of tag chip including Schottky diode should be compatible and require minimum modification in the standard CMOS process. Voltage multiplier is used to convert weak RF signal to DC supply voltage for passive RFID tag chip. The Schottky diodes or CMOS devices in the voltage multiplier chain require finite turn-on voltages in the range of tens mV to hundreds of mV. Because a RFID reader system usually has sufficient sensitivity, the maximum reading range is limited to the distance where the tag chip can receive enough power to turn on these devices [2]. Thus, Schottky diode is the key element in the design of RFID tag.

In this paper, we present the characteristics of the Schottky diodes fabricated using Titanium (Ti/Al/Ta/Al)-Silicon (n-type) junction in 0.35 µm CMOS process, and the effect of the size of Schottky diode on the turn-on voltage and the input impedance of the voltage multiplier was investigated. Based on the measured results of the Schottky diodes, we have designed and tested two key building blocks for UHF-band RFID tag, high efficiency voltage multiplier, and ASK demodulator. We also propose architecture for the tag clock generator with digital calibration that allows the transfer of the precise RFID reader timing information to the tag. Finally, an analysis for long-range RFID tag design considering the limitation caused by the turn-on voltage of tag chip is presented.

II. RFID READING RANGE ANALYSIS

Figure 1 shows a block diagram of RFID tag using backscatter modulation. The tag consists of tag antenna and tag chip. The tag chip includes analog block (voltage multiplier, ASK demodulator, power-on-reset, system clock generator, and modulator), digital block, and non-volatile memory. The input impedance of the tag chip, Z_{in}, is determined by the parallel connection of the voltage multiplier, modulator, and demodulator.

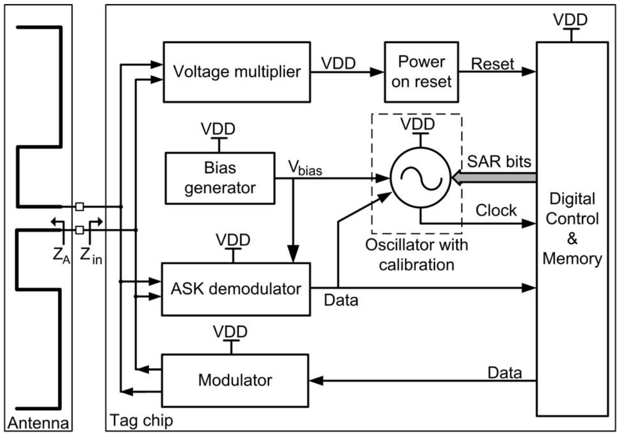


Fig. 1. UHF-band RFID tag consisting of antenna and chip.

Figure 2 shows the equivalent circuit of the RFID tag, where V_{OC} is the open-circuit voltage of the tag antenna induced by the electromagnetic wave from a reader. The equivalent antenna impedance is $Z_A = R_L + R_A + jX_A$ with $X_A = \omega L_A$, where R_A and L_A are the equivalent radiation resistance and inductance of the antenna, respectively, and R_L represents non-radiating antenna resistance and loss from interconnecting antenna to tag chip. The voltage multiplier, whose equivalent circuit is represented by the parallel connection of a resistor, R_{in}, and a capacitor, C_{in}, dominates the input impedance of the tag chip, Z_{in} [3]. For given *EIRP*

(Effective Isotropic Radiated Power), reader antenna gain, G_{read}, and distance r, the peak open-circuit voltage V_{oc} is obtained as

$$V_{OC} = \frac{\lambda\sqrt{8 \cdot R_A \cdot p \cdot EIRP \cdot G_{tag}}}{4\pi r}, \tag{1}$$

where G_{tag} is the gain of the tag antenna under polarization matching condition, λ is the wavelength, and p is the polarization mismatch factor. Then, the magnitude of input voltage to the tag chip, $|V_{in}|$, can be written using the equivalent circuit of Fig. 2 as

$$|V_{in}| = |V_{OC}| \frac{R_{in}\sqrt{1+Q_{tag}{}^2}}{\sqrt{[R_{in} + R_A(1+Q_{tag}{}^2)]^2 + [\omega L_A(1+Q_{tag}{}^2) - Q_{tag}R_{in}]^2}} \tag{2}$$

where $Q_{tag} = \omega R_{in} C_{in}$ is the quality factor of the tag chip by using the general definition of quality factor Q= [ω.(energy stored)/(average energy dissipated)].

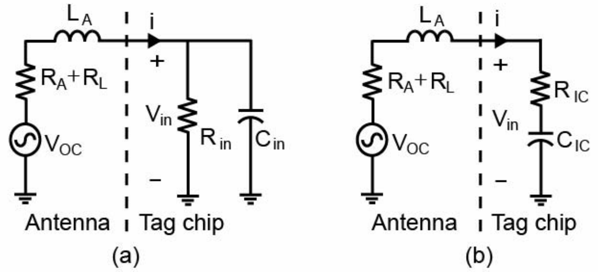


Fig. 2. (a) The equivalent circuit of the RFID tag antenna and tag chip with parallel RC, (b) The equivalent circuit of the RFID tag antenna and tag chip with series RC.

The conjugate-matched condition between the tag antenna impedance and the tag chip input impedance is achieved with the selection of

$$R_A + R_L = \frac{R_{in}}{1+Q_{tag}^2} \text{ and } L_A = \frac{R_{in}^2 C_{in}}{1+Q_{tag}^2}. \tag{3}$$

Under the condition, the tag chip voltage $|V_{in}|$ becomes

$$|V_{in}| = \frac{|V_{OC}|}{2}\sqrt{Q_{tag}^2 + 1}. \tag{4}$$

The above equation shows that high quality factor of tag chip is desirable for providing high turn-on voltage to the tag chip for increased read range. A trade-off is usually required between the maximum Q factor for the chip and bandwidth of proper impedance match. Most of commercial chips available these days have high Q factor (>10) to lower the required turn-on voltage of the tag chip.

For an RFID reader having good sensitivity, the minimum turn-on voltage of the tag chip ($V_{on,min}$) determines the maximum reading range. When this is the case, the detection distance, r_{tag}, for given $V_{on,min}$ of tag chip is obtained by using (1) and (2) as

$$r_{tag} = \frac{\lambda \cdot \sqrt{8 \cdot R_A \cdot p \cdot EIRP \cdot G_{tag}}}{4\pi \cdot V_{on,\min}} \cdot \sqrt{1+Q_{tag}{}^2} \cdot \frac{R_{in}}{\sqrt{[R_{in} + (R_A+R_L)(1+Q_{tag}^2)]^2 + [\omega L_A(1+Q_{tag}^2) - Q_{tag}R_{in}]^2}} \tag{5}$$

Using (5), we can analyze the factors affecting the detection distance. The first term is the ratio of the antenna open circuit voltage to turn-on voltage of the tag chip, which is determined by G_{tag} ,R_A, $EIRP$, and, $V_{on,min}$. The second term indicates that high quality factor is desirable for providing high voltage to the tag chip for increased reading range. The third term is the impedance mismatch factor between the tag antenna and tag chip.

III. VOLTAGE MULTIPLIER USING SCHOTTKY DIODES

Figure 3(a) shows the equivalent circuit of the RFID tag antenna and the N-stage Dickson voltage multiplier. Figure 3(b) and 3(c) shows the equivalent circuit of the Schottky diode, where R_S is the parasitic series resistance associated with metal/silicon contact resistance and well resistance, R_j and C_j are junction resistance and junction capacitance, respectively. R_{SUB} and C_{SUB} are the substrate-related components. All the coupling capacitors C_{2N-1} are chosen so that they are shorted at the RF in put frequency [4]. Therefore, the input impedance of the voltage multiplier is a connection of 2N anti-parallel diodes. For a given tag antenna impedance, design of the diode size and the number of multiplying stage would allow proper conjugate match to the antenna impedance. For this purpose, we fabricated and characterized various Schottky diodes having different diode area and finger numbers.

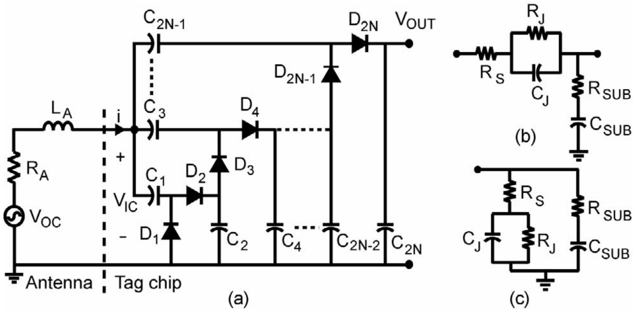
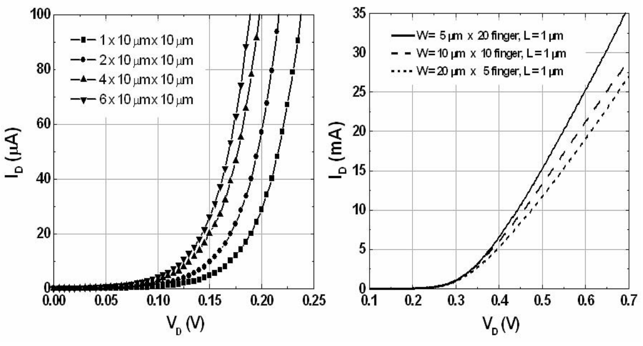


Fig. 3. (a) The equivalent circuit of the RFID tag antenna and the N-stage Dickson voltage multiplier, (b) equivalent circuit model of Schottky diode, (c) equivalent circuit when anode is grounded.

Schottky diodes were fabricated using Titanium (Ti/Al/Ta/Al)-Silicon (n-type) junction in 0.35 μm standard CMOS process. Figure 4(a) shows the measured forward current characteristics of the diode having different sizes. The turn-on voltages for the diode current of 20 μA are 0.19, 0.17, 0.15, and 0.14 V, respectively. The larger the area, the smaller the turn-on voltage for a given current drive requirement, and the efficiency will be higher. However, large capacitance would limit the maximum operating frequency of the multiplier by increasing C_{in}. Design of Schottky diode needs trade-off in saturation current and capacitance determined by diode area [4]. The extracted diode parameters for different sizes are shown in the table, which allows the calculation of the input impedance of N-stage voltage multiplier.



(a) (b)

	1x10x10μm^2	2x10x10μm^2	4x10x10μm^2	6x10x10μm^2
R_j(Ω)	330	297	284	281
$(\omega C_j)^{-1}$(Ω)	505	353	225	167

(c)

Fig. 4. Measured forward current characteristics of the Schottky diode having (a) different number of parallel connected diodes, (b) different unit finger length with the same overall area, (c) measured junction resistance and junction reactance of the Schottky diodes at 900 MHz as a function of diode size at $V_D = -0.3$ V.

Figure 4(b) shows the forward current characteristics of the diode having different unit finger length with the same overall area. The turn-on voltages were almost same for the diodes, but it indicates that short finger length is desirable to reduce the parasitic series resistance. The breakdown voltage was about -9 V, which provides sufficient peak inverse voltage (PIV) necessary for the voltage multiplier in the RFID tag chip.

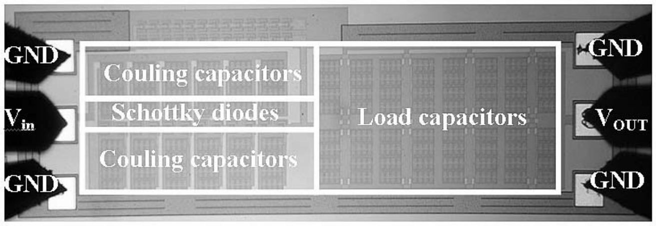


Fig. 5. Photograph of the on-wafer measurement of fabricated 6-stage voltage multiplier. The circuitry area is 1200x300 μm^2 including 64-pF load capacitor.

Figure 5 shows the photograph of the on-wafer measurement of fabricated 6-stage voltage multiplier using Schottky diode. Considering the size of coupling capacitors, each multiplying stage used the Schottky diodes having 10 x 10 μm^2 contact area. The size of coupling capacitors was set to 2 pF, and they were implemented using poly-insulator-poly (PIP) capacitors. To reduce the parasitic resistance, a careful layout including a large number of contacts and multiple metallization was used.

Figure 6 shows the measured results of the voltage multiplier. The output was measured using Tektronics 5510 oscilloscope with input impedance set to 1 MΩ. The 900MHz RF signal was supplied by R&S SMIQ06B signal generator having 50Ω output impedance. The measured input impedance of the multiplier was 13−j26 Ω, which was agreed well with the calculated impedance, 10−j27.5 Ω, from Fig. 4(c). The results show that the multiplier can generate more than 1.5 V with V_{in} of less than 300 mV. With matching network the performance of the multiplier can be improved. The voltage conversion efficiency can be defined as

$$Eff = \frac{V_{out}}{2\times N\times V_{in}}\times 100\ (\%) \tag{6}$$

where V_{out} is the DC output voltage, N is the number of stage. This definition is chosen because ideally the DC output can get to 2N times V_{in}. Because the effect of finite turn-on voltage of the diodes decreases as the input voltage increases, the conversion efficiency becomes better higher input voltage, reaching conversion efficiency of 65% at V_{in}=450mV.

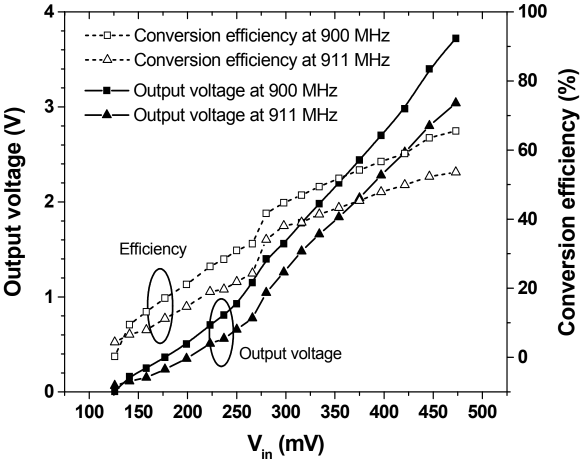


Fig. 6. Measured output voltage and conversion efficiency of the 6-stage voltage multiplier as a function of tag chip input voltage, V_{in}.

IV. ASK DEMODULATOR

Figure 7 shows the circuit schematic of ASK demodulator. The ASK demodulator uses the envelope detection and comparison with the average of the input voltage to recover baseband data. The envelope detector uses the same structure as that of the voltage multiplier with smaller number of stages. The envelope is transferred through a low pass filter to get its average value, and two values are then compared using a comparator. To deal with the voltage ripple from the envelope detector, the comparator needs hysteresis. The envelope detector uses 2-stage voltage multiplier to detect the envelope of the input RF signal. M3, which acts as a resistor, and the capacitor C make the low pass filter. The width and length of M3 determine the resistance.

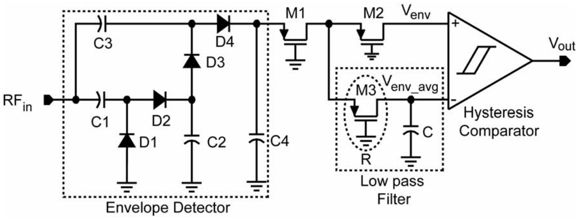


Fig. 7. Circuit schematic of the ASK demodulator.

Figure 8 shows the fabricated ASK demodulator. The measured result in Fig. 9 shows that the ASK demodulator can correctly recover the 900MHz RF signal of peak voltage of about 300 mV.

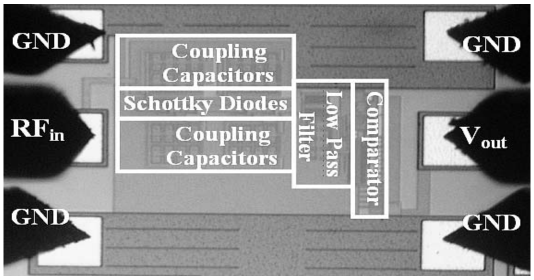


Fig. 8. Photograph of on-wafer measurement of fabricated ASK demodulator. The circuitry area is 300x180 μm^2.

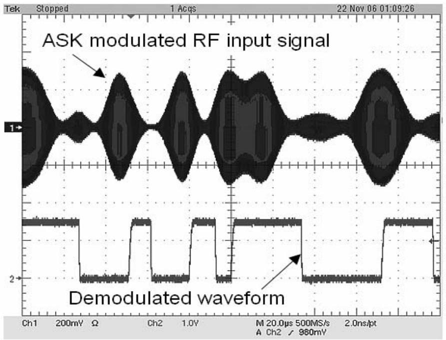


Fig. 9. Measured result of the ASK demodulator. The upper is the RF input signal and the lower is the demodulated output.

V. OSCILLATOR WITH DIGITAL CALIBRATION

Before communicating with a reader, tag adjusts its system clock frequency to 2.2 MHz according to oscillator calibration signal sent by the reader [1]. Because the system clock generated internally using a ring oscillator is susceptible to voltage and temperature variation, it needs digital correction. Figure 10 shows the proposed oscillator with digital calibration and waveform description of its operation. The resistance string (R_0~R_7) in the bias circuit is adjusted by 8-bit binary weighted switched elements, which are controlled by an 8-bit successive approximation register (SAR). The calibration signal consists of eight 116µs-length pulses. A 9-bit counter measures each of these pulses against the output clock of the ring oscillator. Counting pulse and main control signal are generated by the control logic using the reader calibration signal. After an SAR bit is set, the counter starts counting at the rising edge of the counting pulse signal and its MSB is checked at the falling edge of the calibration signal pulse. If the MSB is high, the counter value is greater than 255, so the clock frequency is higher than 2.2MHz, the SAR bit is cleared, else it remains. This process is done in 8 times to collectively tune the system clock to the final frequency of 2.2 MHz ± 0.391%.

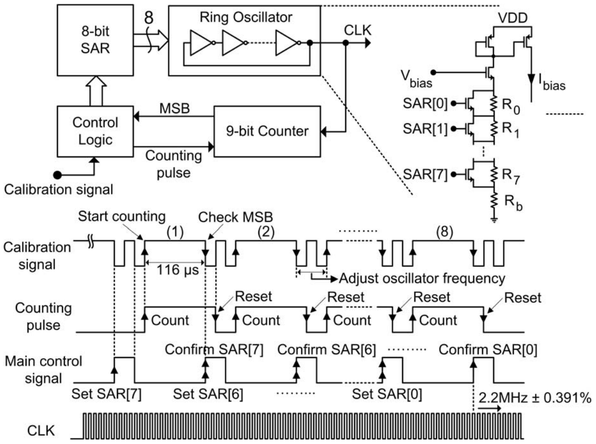


Fig. 10. The proposed oscillator with digital calibration and waveform description of its operation.

VI. CONCLUSION

An analysis and fabricated Schottky diode in standard 0.35 µm CMOS process were presented for implementing the voltage multiplier for long-range 900 MHz RFID system. In addition to the detection range analysis, we presented the design of voltage multiplier, ASK demodulator, and architecture for oscillator with digital calibration.

ACKNOWLEDGEMENT

This work was supported by grant R01-2005-000-11056-0 from Korea Science & Engineering Foundation.

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